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Q. 5.10: A sequential circuit has two JK flip-flops A and B, two inputs x and y, and one output z
Q. 4.25: Construct a 5-to-32-line decoder with four 3-to-8-line decoders with enable and a 2-to-4
Q. 4.8: Design a code converter that converts a decimal digit from the 8, 4, -2, -1 code to BCD
Q. 5.6: A sequential circuit with two D flip-flops A and B, two inputs, x and y; and one output z is

Q. 6.8: The serial adder of Fig. 6.6 uses two four bit registers. Register A holds the binary number

Q. 4.11: Using four half-adders (HDL—see Problem 4.54), (a) Design a full-subtractor circuit incremen

Q. 7.9: A DRAM chip uses two dimensional address multiplexing. It has 13 common address pins, with t

Q. 4.26: Construct a 4-to-16-line decoder with five 2-to-4-line decoders with enable.

Q. 4.5: Design a combinational circuit with three inputs, x, y, and z, and three outputs, A, B and C

Q. 7.8: (a) How many 32K * 8 RAM chips are needed to provide a memory capacity of 256Kbytes? (b) How

Q. 5.18: Design a sequential circuit with two JK flip-flops A and B and two inputs E and F. If E = 0

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